Research Journal of Engineering Sciences ISSN 2278 – 9472
Vol. **2(6),** 25-29, June **(2013)** *Res. J. Engineering Sci.*

Performance Optimization of HVD: An Error Detection and Correction Code

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Available online at: www.isca.in
Received 30th May 2013, revised 11th June 2013, accepted 25th June 2013

Abstract

Several EDAC techniques have been proposed and employed to effectively detect and correct errors introduced during data transmission over a communication channel or at the destination domain during storage. Some of these techniques can detect: only single error, all unidirectional errors, only burst errors, any bit in a data packet is change from one to zero or zero to one it means error is occur in same, errors with known locations assume a code is correct if the error location are known or cannot detect errors which appear in the same location in a pair of message codes. Coding techniques that detects and correct errors are more precise at detecting error locations and correcting them, however if more than one error occur, it becomes a challenge to detect all errors in a data frames and converted back its original form . In this paper, an advanced error detection and correction method to protect against errors is proposed. This method is based on 4D parities checking. This method, which is named HVD, provides very high detection coverage rate that can correct up to three flips in a data bit. The performance of HVD is optimize in comparison with the following coding techniques: CRC, Hamming codes. An independent design platform is utilized for the simulation by Xilinx 8.1 using ModelSim SE-EE 5.4a which shows a significant reduction in uncorrected errors during data transmission. The efficient performance of HVD makes it a more applicable coding technique for communication, data transmission, different protocols and other application.

Keywords: Burst error, CRC (Cyclic Redundancy Check), EDAC (Error Detection and Correction), Hamming Code, HVD (Horizontal Vertical Diagonal), Message bits, Xilinx, ModelSim.

Introduction

In communication systems, data packets can be sending through the channel the contents of packets are protected by an EDAC code. During the transmission of data, generation of error is renowned difficulty in communication and HVD codes have been a reliable solution to this problem. These codes are design with the help of software using extra parity bits and encoder/decoder. In systems where HVD hardware is not available, the consistency of the system can be increased by providing security through software. An advanced EDAC method to guard against soft errors is proposed. This method is based on parities for each row, column and diagonal in slash and backslash directions. HVD provides advanced detection process that can correct up to three changes of bits in a data packet. While the proposed method includes data overhead more than previous methods, however, it improves the error detection and correction exposure using parity codes which have low calculation latency and realization complexity[1].

There are three types of error introduced in the data packet at the channel (transmission path). These are single-bit error, Multi bit error and burst error as shown in figure 1. In a single-bit error, occur when only one bit flip from one to zero or zero to one as shown in figure 2. Multi Bit Error: When two or more nonconsecutive bits in the data unit have changed and finally Burst Error: A burst error means that two or more consecutive bits in the data unit have changed as shown in figure 3.

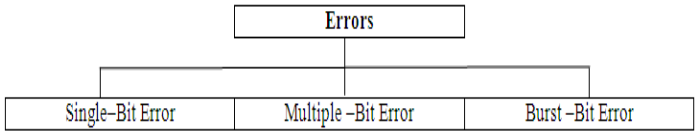

Figure-1
Types of error [2]

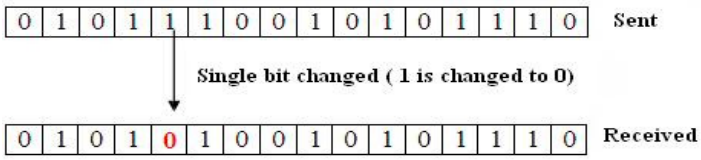

Figure-2
Single bit error [2]

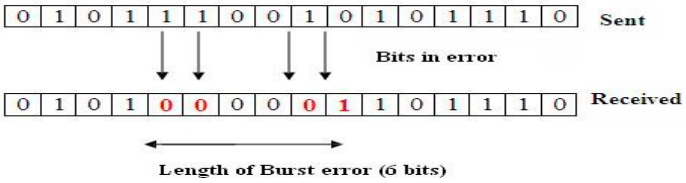

Figure-3
Burst bit error [2]

Correction of error is more complicated than the detection. In error detection, we are check only message bits, error in take place or not. And in error correction, we require the accurate number of bits that are corrupted and more importantly, their location in the message, number of the error and the size of the message [2].

EDAC models are more methodical by introducing extra parity bits to locate the location of the error and correcting them, however for some models if one or more error occurs, it becomes difficult to identify all errors and converted data to its original form correctly. On the other hand there are some models for which the full-duplex mode is not allowed with the presence of errors, for such system, there is no likelihood of a message retransmission, and so the receiver has to realize some error correction algorithm to precisely decode the message. An EDAC code HVD is presented that simultaneously: evaluate the data stream or information, evaluate and detects error codes from the data stream or information. If error occurs, addresses all error positions via the use of extra parity bits and corrects all errors precisely even if more than one error occur in a data packets and finally achieve data verification at the receiver domain. In this paper, the performance of HVD is evaluated in comparison with the following coding techniques: CRC Hamming codes, and An independent design platform is utilized for the simulation by Xilinx 8.1 using ModelSim SE-EE 5.4a which shows a significant reduction in uncorrected errors during data transmission. The efficient performance of HVD makes it a more applicable coding technique for communication, data transmission, different protocols and other application.

The research paper is structure as; section 2 presents the literature review. It covers previous work for EDAC methods, in the section 3; the proposed method of EDAC is described, in the section 4, includes explanations of results and in the section 5 paper is finally concluded.

Previous Works

Clarke, K.P., presented an analytic comparison of checksum coding techniques[3]. McAuley investigated Fletcher checksum and CRC coding methods and proposed the Weighted Sum Codes (WSC) algorithm as an alternative method[4]. Filmier carried out an analytical evaluation of weighted sum code alongside Fletcher checksum, XOR checksum, one's complement addition checksum, and CRC and block parity. He asserted that WSC has high computational speed as Fletcher checksum and error detection capability as CRC[5]. Berrou et al discovered a class of codes termed turbo codes that exhibit near Shannon limit performance by means of iterative decoding algorithms[6]. Baicheva et al[7] and Kazakov[8] examined the efficiency of optimal CRC polynomials for specific lengths. Richardson et al, analysis on coding methods revealed that bit error performance deteriorates as the data bits length decreases in size. Koopman and Koopman and Chakravarty investigated CRC polynomials and proposed a polynomial selection process for embedded networks[9]. HVD presented a error detecting and correction technique, HVD, which generate and add extra bit (parity bit) with the data or message bits and sent through the transmitter and at the receiver end generate parity bit and compare it to the received data.

Methodology

Proposed Method: The proposed EDAC method is called HVD code since the parity bits are applied on the row, column and two diagonals on a data part. In adding to horizontal (H) and vertical (V) parity bits, we use slash diagonal (SD) and backslash diagonal (BSD) parity bits in four directions as shown in figure 4.In order to enhance the detection capacity, an added parity bit is calculated based on designed parity bits of each dimension. In our HVD code realization, in a matrix (h, v, sd, bsd) respectively. A. Error Detection Method as well as B. Error correction method.

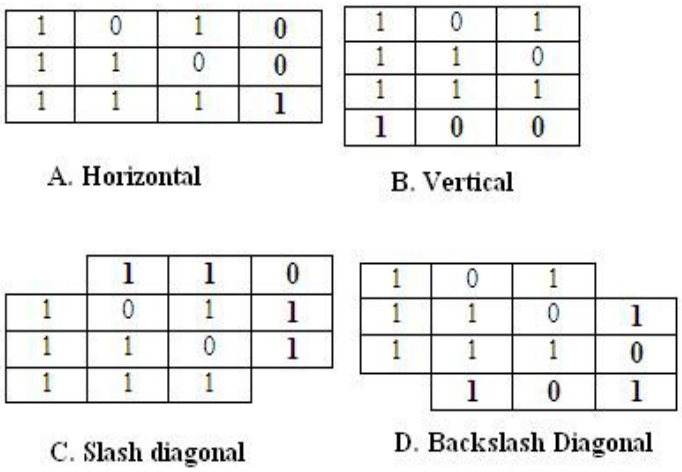

Figure-4
The horizontal, vertical, slash and backslash diagonal dimension parity scheme in HVD

Detection Method: For the data packet, parities bits are computed in all the directions (H, V, SD, and BSD) at the destination (for example, from v_1 to v_8 in vertical direction). These computed parities are evaluated against the actual received parities. If the result of evaluation does not specify any change in a data packet, it means the received data at the destination is correct, no need of correction ; but if there is a distinction between the received and computed parities, the erroneous parity lines are recognized and then the correction procedure starts. This property is useful in real-time and high speed applications.

Correction Method: At the end of the detection procedure, the error parity position are marked with a round as shown in figure 5.For correction, first the applicant bits are marked. Wherever atleast two of the four error parity lines interconnect, that bit in array is marked as applicant bit. Applicant bits for the error parity lines are shown with black square in figure 6.

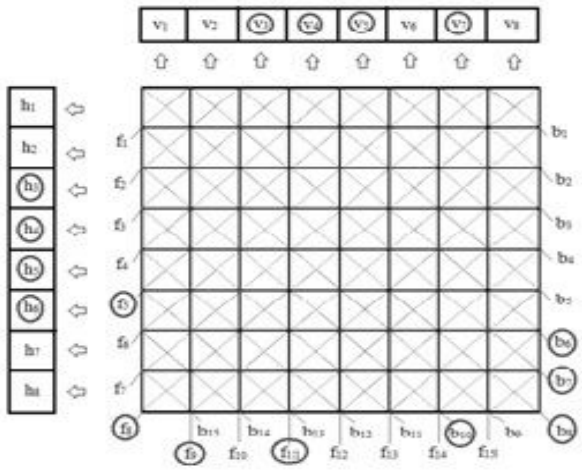

Figure-5
Coded array with erroneous parities

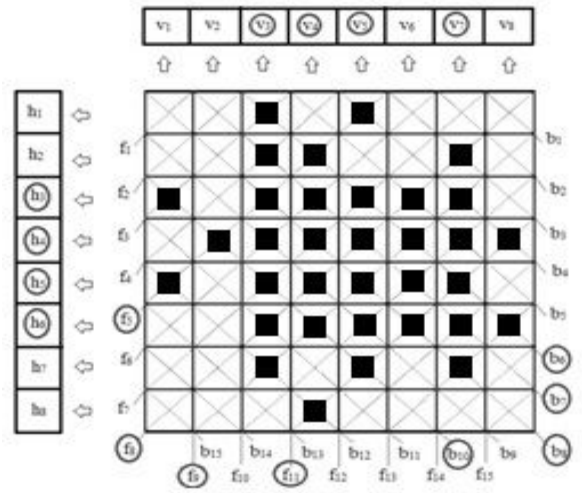

Figure-6
Coded array with data bits

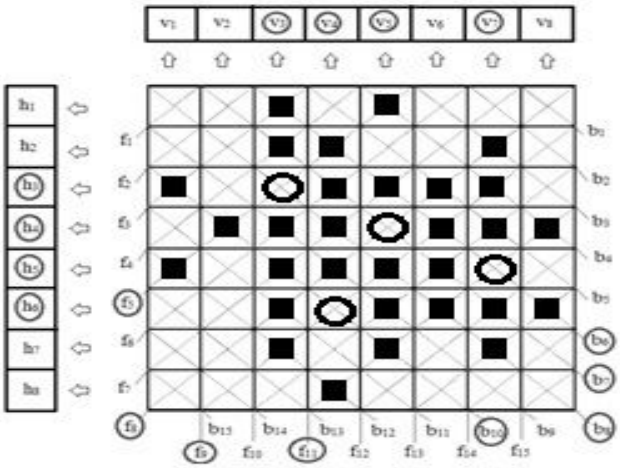

Figure-7
Coded array with error bits

To find the error bits among the applicant bits, all the applicant bits are checked. The applicant bit for which all the four lines interconnect, is an error bit; if not then the bit is correct. This particular applicant bit can be removed. The error bits for the set of applicant bits in figure 6 are shown with dark round in figure 7.These error bits are flipped to correct.

To find whether the error bits are data bits or parity bits, the error bits can be checked as, if the position of the error bit is 2^k (for k = 0, 1, 2, 3….), then it is an erroneous parity bit otherwise it is a data bit that is error.

Results and Discussion

Result: This method is simulating in Xilinx 8.1 using ModelSim SE-EE 5.4a platform and the strength of the method is calculated by random error amalgamation. The results show that, an enormous arrangement of various errors can be corrected. The number of errors that can be corrected depends upon the length of the array of coded word. It enhance with the length of the array.

Percentage of Redundancy: To detect or correct the error we have to use some extra bits. These extra bits are called redundancy bits. We add these redundancy bits to the information data at the source end and remove at destination end. The simulation results shows that a small increase in the number of parity bits can cause an increase in number of data bits that can be transmitted as a whole codeword as shown in figure 8.

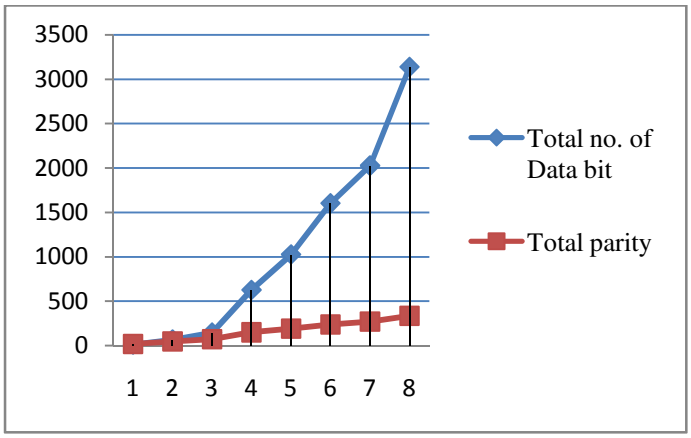

Figure-8
Variation in redundant bits

Code Rate: The code rate can be defined as; "the measure of relative amount of information which is transmitted in each codeword" .It is an important metric to evaluate the performance of any error detecting and correcting code. For a good error detection and correction method should have more code rate. In The variation in code rate for different bits is shown with blue line in figure 9[2].

Code Rate = (R) =Data Bits (k)/ Total number of bits (n)

Where k is data bits and n is total number of bits in the codeword.

Bit overhead: Another important measure to compare the two codes is the bit overhead. The bit overhead (BO) can be defined as, "the ratio of parity bits to data bits". Bit overhead determines the percentage of redundancy in the codeword. A good EDAC method should have lesser bit overhead. With the proposed method, we can get the reduced bit overhead as shown with red line in the figure 9[2].
Bit Overhead = BO = Parity bits (c) / Data bits (k)

Simulation Result: The VHDL codes for correction function are simulated for various lengths of code such as 4, 9, 16, 32 and 64 bit code. Simulation result, error is high (at the receiver end) is given in figure 10. The simulation results after EDAC in a 3x3 data array is given in the figure 11.

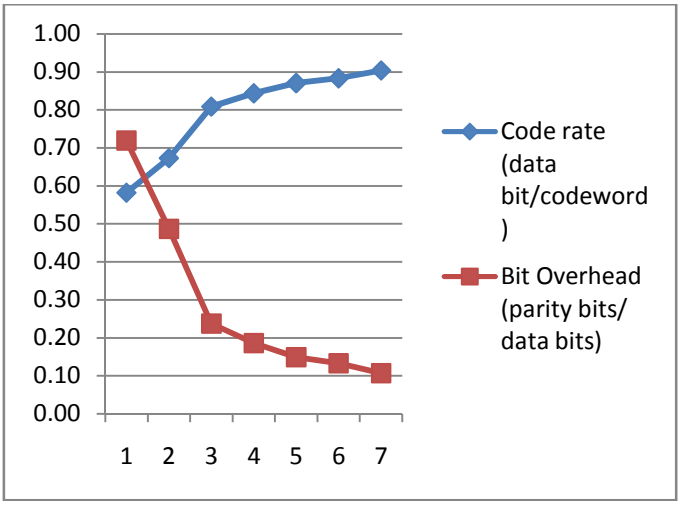

Figure-9
Code rate and Bit overhead for various bits

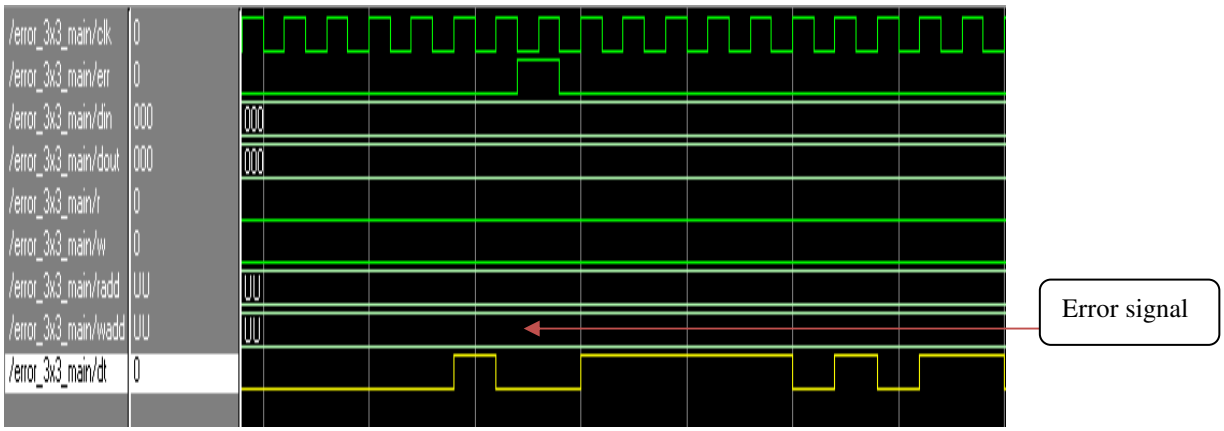

Figure-10
Simulation result when error signal is high

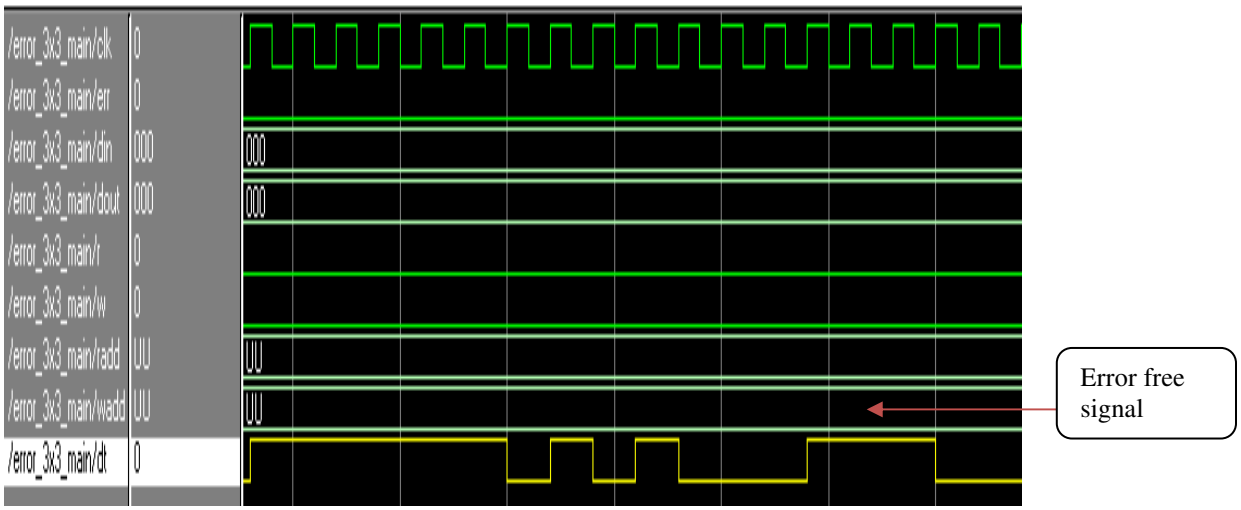

Figure-11
Simulation result for correction function

Conclusions

In this paper a simple method with smaller calculation is presented. It is a painless method of detecting the errors by amputation of error bits, so it can be remove complexity of the circuit. With the help of method can detect and correct the errors in data bits as well as in the parity bits without any extra calculations. This paper presents an advanced EDAC method which is entitles as HVD code. This kind of detection and correction code uses the parity code in 4D in a message. Any change of bit in a data packet can be detected and two or three bit errors can be corrected, depend on the experimental results

References

1. Anlei Wang, Member, IEEE, and Naima Kaabouch, Member, IEEE. "FPGA Based Design of a Novel Enhanced Error Detection and Correction Technique, 25-29 **(2008)**

2. Behrouz A. Forouzan Data Communication and networking, 2nd edit. Tata McGraw Hill **(2011)**

3. Clarke K.P., Reed-Solomon error correction, Research and development British Broadcasting Corporation, WHP 031 BBC **(2002)**

4. McAuley A.J., Weighted sum codes for error detection and their comparison with existing codes, *IEEE/ACM Trans. on Networking,* **2(1),** 16–22 **(1994)**

5. Feldmeier D.C., Fast Software Implementation of Error Detection Codes, *IEEE/ACM Trans. Networking,* **3(6),** 640-651 **(1995)**

6. Berrou, C., Glavieux A. and Thitimajshima P., Near Shannon limit error-correcting coding and decoding: Turbo-codes International Conference on Communications, 1064-1069 **(1993)**

7. Baicheva T., Dodunekov S. and Kazakov P., On the cyclic redundancy-check codes with 8-bit redundancy, *Computer Communications,* **21,** 1030–1033 **(1998)**

8. Kazakov P., Fast calculation of the number of minimum-weight words of CRC codes, *IEEE Transactions on Information Theory,* **47(3),** 1190–1195 **(2001)**

9. Koopman P., 32-bit cyclic redundancy codes for internet applications, in International Conference on Dependable Systems and Networks, June 23–26, 459–468 **(2002)**

10. Mostafa Kishani, Hamid R. Zarandi, Hossein Pedram, Alireza Tajary, Mohsen Raji and Behnam Ghavami, HVD: horizontal-vertical-diagonal error detecting and correcting code to protect against with soft errors, **(2011)**